REMARKS

Claim Rejections – 35 U.S.C. 103(a)

Claims 1 – 3, 7 – 9, 12 and 14 were rejected under 35 U.S.C. 103(a) as being unpatentable over Shim in view of Romano et al. and Yuen et al.

Response

Claim 1

The Examiner stated that the memory controller recited in Claim 1 is anticipated by Shim's memory controller (508), which is shown in Shim FIG. 5. The applicant respectfully disagrees.

In col. 5, lines 53 – 62, Shim explicitly states: "Namely, the memory controller 508 reads data to be descrambled from the memory 320 and/or allows the memory 320 to buffer the descrambled data and transfer the buffered data to the audio and video decoders 620 and 630 or the ROM decoder 950 according to the data transfer control signal generated from the microcomputer 500. The audio and video decoders 620 and 630 or the ROM decoder 950 generate a transfer request signal A/V_RD, so as to cause the microcomputer 500 to generate the transfer control signal to the memory controller 508" (*emphasis added*). Therefore, the audio decoder and video decoder (620, 630, FIG. 5) taught by Shim only request data from the memory (320, FIG. 5) for completing the desired audio/video decoding process by issuing a transfer request signal (i.e. a read request); however, Shim fails to teach or suggest that the decoding result generated from the audio/video decoders (620, 630, FIG. 5) is written back to the memory (320, FIG. 5) for data buffering. In other words, the applicant points out that the memory controller taught by Shim **only provides read access** to the memory for the audio/video decoders, which can be seen from Shim FIG. 5 showing that the data path, represented by a thick

arrow symbol pointing to the audio/video decoders from the memory controller, allows a one-way data transmission only. In contrast to the cited memory controller taught by Shim, the claimed memory controller is defined to provide **read and write access to the external memory** for both the servo control and ECC decoder circuit **and the graphics decoding circuit**. The memory sharing architecture taught by the applicant is different from that implemented in Shim's system. The applicant therefore asserts that the claimed memory controller is not anticipated by the teachings of Shim.

In addition, the applicant asserts that Yuen and other cited prior arts fail to teach "*the servo control and ECC decoder circuit further comprises a register* ***accessible by the graphics decoding circuit that indicates the location of decoded data in the external memory.***" as recited in the claim1. The directory controller taught by Yuen is unrelated to the present invention and the applicant finds no evidence of Yen teaching *a register* ***accessible by the graphics decoding circuit that indicates the location of decoded data in the external memory***.

In view of the above reasons, Claim 1 should be found allowable over the combined teachings of Shim, Romano and Yuen. Withdrawal of the rejection and reconsideration of Claim 1 are respectfully requested.

Claims 2 – 3 and 7 – 9

Claims 2 – 3 and 7 – 9 are dependent on Claim 1 and should be found allowable if Claim 1 is found allowable.

Claim 12

Claim 12 similarly claims the memory controller used to provide read and write access to the external memory for both the servo control and ECC decoder circuit and the graphics decoding circuit, as claimed in Claim 1. As fully detailed in the response to

Claim 1, the applicant believes that the combined teachings of the cited references.

In addition, the applicant asserts that Yuen and other cited prior arts fail to teach the following:

the servo control and ECC decoder circuit further comprises:

a first register indicating a first storage location in the external memory for the encoded data from the removable media;

a second register indicating a second storage location in the external memory for the decoded data which is decoded from the encoded data; and

a third register indicating a size of the decoded data.

The directory controller taught by Yuen is unrelated to the present invention and the applicant finds no evidence of Yen teaching *a register* ***to indicate the first storage location for the encoded data, a second register to indicate the second storage location for the decoded data, and a third register to indicate the size of the decoded data.***

Therefore, the applicant believes that Claim 12 should be found allowable. Withdrawal of the rejection and reconsideration of Claim 12 are respectfully requested.

Claim 14

Claim 14 is dependent on Claim 12 and should be found allowable if Claim 12 is found allowable.

Claim 6 was rejected under 35 U.S.C. 103(a) as being unpatentable over Shim in view of Romano et al. and Yuen et al. and further in view of Cho.

Response

Claim 6 is dependent on Claim 1 and should be found allowable if Claim 1 is found allowable.

Claims 15 – 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Shim in view of Romano et al. and Yuen et al. and further in view of Iwamura.

Response

Claims 15 – 17 are dependent on Claim 12 and should be found allowable if Claim 12 is found allowable.

Patentability of New Claims 18 and 19

Claims 18 and 19 are newly added and include limitations fully supported by FIG. 2 and pertinent description in the specification of applicant's disclosure. No new matter is introduced. Consideration of the claim amendments is respectfully requested.

In the Office action dated 02/08/2008, the Examiner stated that Shim, FIGS. 4 and 5 show a communications pathway between the servo control (400) and ECC decoder circuit (210) and the graphics decoding circuit (620, 630). The applicant notes, however, that circuit (210) comprises an ECC circuit (230) and a memory controller (508) as shown in FIG.5, and FIG.5 shows that the graphics decoding circuit connects with the memory controller and not the ECC circuit. Communication between the graphics decoding circuit and the servo control and ECC decoder circuit is therefore only possible through the memory controller. Moreover it should be noted that the connection through the demultiplexer is also not illustrated as a direct connection between the graphics decoding

circuit and the servo control and ECC decoder circuit. Shim only teaches that the memory controller is for controlling access to the memory, and neither teaches nor suggests that there is a communications pathway between the servo control and the graphics decoder. Furthermore, the applicant contends that such an implementation is not obvious, as the claimed connection between the graphics decoding circuit and the servo control and ECC decoder circuit is defined for enabling the information decoded by the ECC decoder circuit to be correctly stored in the memory, and information needed by the graphics decoding circuit to be correctly located. As the connection between the graphics decoding circuit and the servo control and ECC decoder circuit as taught by the prior art is through the memory controller, the communications pathway for enabling the graphics decoding circuit to locate data therefore becomes redundant.

In the Office action dated 02/08/2008, the Examiner has also cited the directory controller of Yuen as reading on the claimed feature directed to the register accessible by the graphics decoding circuit. The applicant respectfully disagrees. Yuen teaches a removable media (the videotape) but does not teach an external memory. Claims 18 and 19 define that the graphics decoding circuit can access the register of the servo control and ECC decoder circuit to directly access a location in the external memory for decoding the data stored in said location. As the teachings of Yuen relate to videotape media, utilizing the directory controller for finding a location in the videotape and generating graphics and audio data corresponding to data in said location would necessitate the use of the servo control circuit to physically move the videotape to the desired location. Therefore, the utilization of the memory controller for enabling direct access of the external memory by the graphics decoding circuit becomes redundant, as the graphics decoding circuit would still have to utilize the servo control-memory controller connection for accessing the memory.

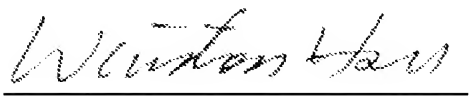
As both Yuen and Shim fail to provide adequate reasoning for including inter-communication between the two circuits, Shim fails to teach a direct connection

between the two circuits and Yuen further fails to teach the direct accessing of the external memory by the graphics decoding circuit as claimed in Claims 18 and 19, the applicant contends that Claims 18 and 19 should be found allowable over the cited references. In addition, Claims 18 and 19 are dependent on Claims 1 and 12 respectively, and should be allowed if Claims 1 and 12 are found allowable.

Conclusion:

Thus, all pending claims are submitted to be in condition for allowance with respect to the cited art for at least the reasons presented above. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,



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Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)